**Experiment-1 : 4x1 Multiplexer**

**Objective:**

To design a 4x1 Multiplexer and write a simple test bench for it. The test bench should generate stimulus to completely verify the functionality of the design under test with delay of 20ns.

**Theory:**

Multiplexer is a combinational circuit that has maximum of 2n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines such that, each combination will select only one data input.

**DUT Code:**

//Design

module mux(input [3:0]i, [1:0]s, output y);

    assign y = s[1]?(s[0]?i[3]:i[2]):(s[0]?i[1]:i[0]); //logic for mux

endmodule

**TB Code:**

//TB

module mux\_tb;

    reg [3:0] i;// Input of mux

    reg [1:0] s; //select line of mux

    wire y; // output of mux

    integer x = 0; // integer to count error

    mux uut(i,s,y); //instantiation

    initial begin

        repeat(10)begin //test 10 times

            i = $random; // random input (4 bits)

            s = $random; // random select input (2 bits)

            #20; //20 ns delay as mentioned in exp requirement

            if (y != i[s]) x = x + 1; //check if y is mapped to correct input

        end

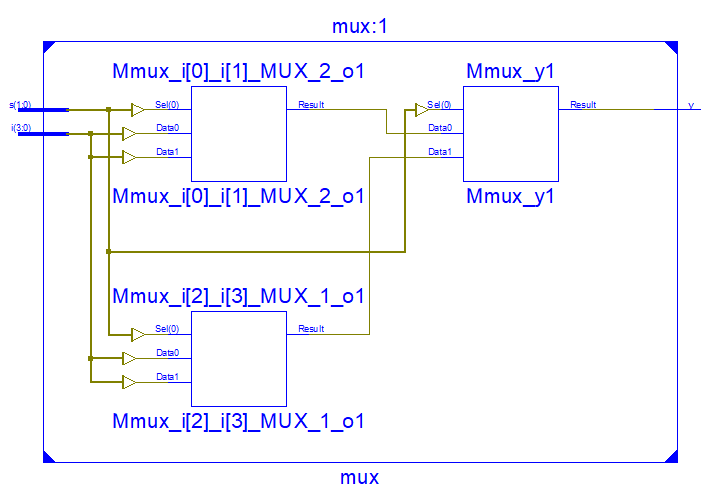
        if(!x) $display("Success"); //print success when no loop raises error

        else $display("Failure"); // else print failure

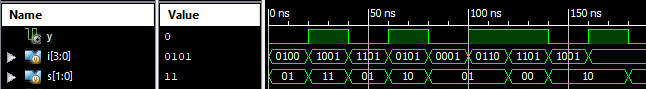
    end

endmodule

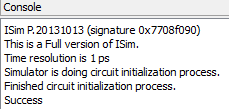
**RTL Diagram:**

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**Output Waveform:**

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**Simulation Output:**

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**Result:**

The simulation output and the RTL diagram is observed and found to be valid.